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Percival soft X-ray CMOS Imager for Photon Science – Status and Prospects

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Abstract.
Percival is a CMOS-based imager with 2 megapixels, also called P2M, designed for photon science experiments. The first generation of the P2M sensor showed some performance issues. Specifically, ADCs in full-speed operation mode are affected by crosstalk and show a non-linear and uncorrectable response. A firmware hack to the readout and data acquisition system has been introduced to partially overcome these effects, at the cost of limiting the frame rate to 83 Hz. Moreover, a non-uniform dark response of the sensor pixels is observed, explained by non-uniform bias currents across the chip: two opposite edges of the sensor cannot be digitized when applying biases that have the centre of the sensor operating normally. These issues are addressed in the re-submission of the chip. In this contribution, we present the current status of the detector and the first results from the re-designed sensor.

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1 Introduction

Percival detector or P2M has been designed to detect soft X-rays in photon-science experiments [1]. Some of the features of Percival are as follows: pixel pitch size of 27 μm covering an area of 38 mm $\times$ 40 mm, design frame rate of 300 Hz for the full frame size (faster in Region of Interest or ROI operation), and a dynamic range from single photon to 50000 photons per pixel per frame (for photon energy of 250 eV). These specifications are achieved by the parallel readout of the chip (7+1 Analog to Digital converters for each column) and the adaptive gain per pixel (3 gain modes). Backside processing (thinning and passivation) renders the detector sensitive to soft X-rays. With the first generation P2M, images down to 70 eV have been recorded at FLASH [2]. First successful user experiments with the prototype sensor were performed on FLASH and PETRA beamlines in 2020-2023. The first generation of P2M showed two main issues: 1. Due to the crosstalk, the ADC output as a function of input voltage showed a non-linear behaviour; 2. Due to a non-uniform current across the chip, the dark image showed a non-uniform response, also known as the "bathtub effect". A thorough explanation of the cross-talk issue has been presented in [3]. A summary of these solutions is given below.

To overcome the crosstalk issue for optimum noise, the first generation chip has to be operated in an interleaved mode where half of the rows across are not read out. In addition, the ADC conversion phase has to be separated from the rest of the readout or work in a "Sequential" mode. This is necessary because the crosstalk effect in the "Full-Speed" mode, where ADC conversion is done in parallel, makes the ADC calibration impossible. In the sequential mode, the frame rate was limited to a maximum of 83 Hz (an integration time of 12 ms).

The "bathtub" effect causes a non-uniform baseline across the chip. As a result, pixels at the chip boundary show a higher ADC response than the pixel in the middle. The effect becomes more evident at the higher gain and effectively makes those pixels unusable at the highest gain mode. To avoid this issue, the 1st-generation sensor was either operated in the highest possible gain without gain switching (thus adding a bit of headroom to the ADC conversion and increasing the usable area in the highest gain), or in multi-gain operation starting from lower amplification and a correspondingly higher noise threshold. After observing these issues, a second version of the chip, known as "respin", was designed and submitted to the foundry. For the cross-talk issue, a shielding has been added between the data and control lines to protect the ADC data. For the bath-tub effect, the homogeneity of ground across the top of the matrix was improved by detaching the edge ground connection. The chips from the second production were processed, wire-bonded and delivered to the lab for characterisation this summer.

In this contribution, we present the first preliminary results of the measurement with the respin chip and a comparison with the first generation chip. After the introduction, in Section 2 a summary of the P2M system in the lab is given, in Section 3 the results of the characterisation of the respin chip are given and a conclusion is given in Section 4.

2 P2M system

Percival detector is a monolithic active pixel sensor, manufactured in a commercial 180 nm technology [4]. The imaging area has 1484 $\times$ 1408 pixels. Each pixel includes a photodiode and three capacitors which allow the sensor to work in an adaptive gain mode. This mode increases the dynamic range of the sensor, as discussed in the introduction.

Foundry provides us with Front Side Illuminated (FSI) chips, only. Due to a layer of SiO_2 and traces of metal, low-energy photons do not reach the sensor. Therefore, we need back-back-side illuminated (BSI) wafers and a back thinning process in order to be sensitive to soft X-rays.

The readout of the sensor is done as follows: 7 rows are read by 7 ADCs at the end of each column simultaneously and an 8th ADC is available as a spare. The ADC in the P2M chip is a ramp ADC which digitises the signal to coarse (most significant value) and fine (least significant value) bits with 5 and 8 bits, respectively. In addition, there are 2 gain bits. In total, 15 bits are produced for each pixel. The data is transmitted from the chip with 45 Low Voltage Differential Signaling (LVDS) lines. Each LVDS line works for 32 columns and each column contains 7 ADCs blocks. In total, a packet with 3360 ($7 \times 32 \times 15$) bits is sent out by a single LVDS line. This data is serialized by an on-chip serializer.

The ASIC is connected to a Low Temperature Co-fired Ceramic (LTCC) board which brings the the electrical signals to a set of connectors. To bias the chip and monitor the voltages and currents, a dedicated power board has been developed. This board provides 24 bias voltages and 21 bias currents which can be controlled and monitored, independently.

The cables, which transport LVDS signals and I2C information from the LTCC, are connected to a so-called carrier board which is responsible for controlling the chip as well as Data Acquisition (DAQ). For controlling the chip, a Virtex-6 FPGA is used on the carrier board. For DAQ, the carrier board hosts a DAQ board also known as the Mezzanine board. The mezzanine board is responsible for preparing the data in a User Datagram Protocol (UDP) format and sending it out using two optical fibres each working at a maximum speed of 10 Gb/s. The data from the mezzanine is then transferred to Linux clusters through a deep buffer switch.

3 Results

In the following, the results of the measurements with two respin P2M heads, one FSI head and one BSI head, in the lab are presented. The results are shown in three sections:

- ADC ramp measurements for FSI heads which are used to evaluate the crosstalk effect (we have not seen any differences between crosstalk of FSI and BSI chips).
- Measurement of average ADC coarse values as a function of column index used to evaluate the bathtub effect in BSI heads.
- Noise measurement at standard operating temperature ($-20\,^{\circ}$C).

For the cold measurements, the detector head was placed inside a vacuum chamber. It should be noted that in the case of the respin BSI head, half of the sensor (columns 0 to 704, corresponding to one ADC/periphery stitching block) was responding. Therefore, the results shown for the respin BSI head include only pixels from the functioning half.

3.1 ADC ramp measurement

As discussed in the introduction, due to the crosstalk effect, ADC showed a non-linear behaviour for the first generation heads. One way to visualise this effect is to take ADC ramp data in which the input of the ADC is provided by a known voltage (instead of the photo-diode) and the ADC output, i.e. fine and coarse bits, is read out. Ideally, for a perfectly linear two-ramp ADC, this should result in a series of linear ramps. The following results were taken at room temperature and similar bias conditions for two FSI chips, a first generation chip (FSI01) and a respin chip (FSI13).

Fig. 1a shows this data for one pixel in a first generation FSI chip in two modes of operation. One identifies a plateau region where fine bits do not increase as a function of the input signal, especially in the full-speed mode. This response makes the ADC calibration impossible (since a wide range of range of input voltages results in identical ADC output) and in turn, increases the noise of the chip. Fig. 1b shows the same plot for a respin FSI chip. A clear improvement in ADC linearity is visible for both modes of operation. From these results, it is clear that the crosstalk effects have been reduced in respin chips, and the respin chip can be operated in both sequential and full-speed modes. The remaining non-linearity in the full-speed mode (around fine values of 150) can be corrected by a non-linear ADC calibration based on the lookup tables.

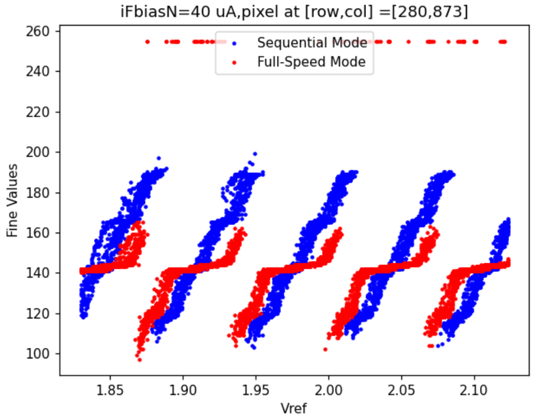
3.2 Dark image uniformity (the pre-respin "bathtub effect")

As discussed in the introduction, in the first generation of P2M, the dark image shows a severely non-uniform response for BSI heads, especially in the very high gain mode. This "bathtub effect" makes the pixels placed at two opposite edges unusable and limits the dynamic range of the detector. One way to characterise the bathtub effect is to take a dark image and plot the average coarse bits as a function of the column index. The headroom between the coarse value of the dark image and the maximum coarse value gives an index of the bathtub effect. A large headroom means the effect is less severe.

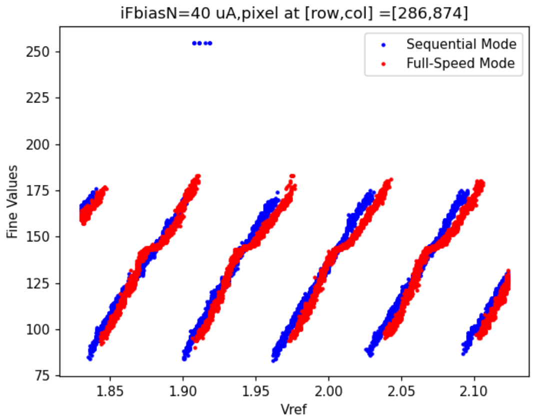
Fig. 2 shows this plot for first and second-generation chips. One can clearly recognise a flatter response for the respin chip which means the bathtub effect has been reduced in this version of the chip. Therefore, one can use the very-high gain mode without excluding the pixels at the boundary. It should be noted that by changing the bias settings, one can tune the location of baseline towards higher or lower values. Thus the fundamental change from the respin is the changed "slope" of the blue (respin) vs red (the first generation) sensor. The grey curve (labeled as "operational mode") in Fig. 2 shows the result for an optimized bias setting for the chip which maximize the "headroom" towards higher coarse values. The blue shaded area shows the region in which the chip can be operated, i.e. the headroom for the signal.

3.3 Noise measurement

Noise is one of the most important features of a photodetector which affects the lowest photon energy it can detect. To determine the noise for the P2M, the detector head was placed in a vacuum chamber and cooled down to $-20\,^{\circ}$C. First, the ADC calibration was performed at $-20\,^{\circ}$C which determines the calibration constants for all pixels for both sample and reset images. Then, a series of dark images (1000



(a) FSI01 (First generation chip)



(b) FSI13 (Second generation chip)

Figure 1: ADC ramp measurements for a pixel in a first (a) and a second(b) generation chip.

frames) was taken in the very high gain mode for a given integration time. Using ADC calibration results, the dark images were converted to an Analog Digital Unit (ADU). Then, the standard deviation of 1000 dark images was calculated for each pixel yielding the noise in ADU.

To convert the ADU to electron, one needs first to measure the gain (e/ADU) of the detector using the Photon Transfer Curve (PTC) technique. This technique is described in detail in [5] and requires taking images while the detector is illuminated with a constant light source and then changing the intensity of the light or the integration time of the chip. We have used an array of LEDs with red light (wavelength of 660 nm as the light source). The average gain across the pixel matrix was found to be around 1.65 e/ADU for the very high mode. It should be noted to reduce the statistical fluctuations, the average gain of two adjacent pixels in the same row is calculated (rather than calculating the gain for each pixel). Fig. 3 shows the gain map for the respin head.

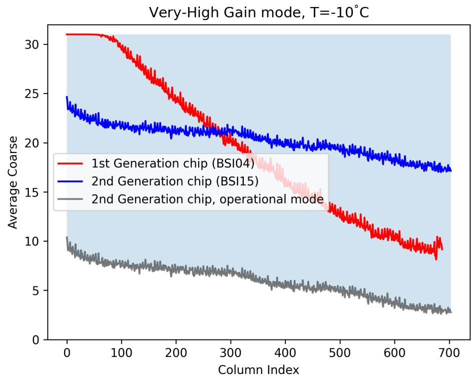


Figure 2: Mean coarse bit as a function of column index for a first and second generation chip. The grey curve shows the curve for the respin chip after adjusting the bias setting for an operational mode. The plots are shown for half of the chips because pixels at half of the respin chip (col 0-704) were responding. The blue shaded area shows the headroom for the signal.

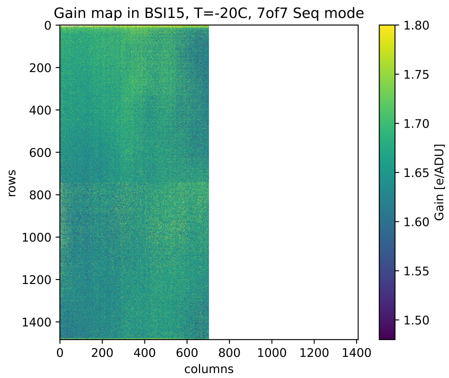


Figure 3: Gain [e/ADU] map the BSI respin chip measured at $-20\,°$C.

The noise in electrons is simply calculated by multiplying the noise in ADU for each pixel by its gain. Fig. 4 shows the noise spectrum for the BSI chip. The average noise for all pixels in the chip (in its functioning half) is 12.6 electrons. This number is similar to the noise measured for the first generation chip reported in [3] when it was operated in the interleaved mode where half the rows are not read and pixels at the boundary (columns 0-350 and 1100-1408) were excluded due to the bathtub effect.

4 Summary and Conclusion

In this paper, we presented the first results of lab measurements with respin Percival chips. The results of the measurement with the FSI chip show a clear improvement in the crosstalk issue seen in the first generation of the chip. It was shown that this improvement leads to a better linearity of ADC blocks in both parallel and sequential modes. The results of the measurements with the BSI respin head show a better bathtub uniformity in dark images. This improvement enables us to use the highest gain in dynamic operation. The noise measured for the BSI respin head is comparable to what was measured for the first generation chip when it was operated in the noise-optimised interleaved mode where half the rows are not read and the pixels at the boundary are excluded.

In conclusion, the respin P2M head has provided a solution for key issues seen in the first generation P2M successfully and shows a vastly improved performance. Therefore, Percival can now be used for a wider range of applications,in particular also in cases needing noise performance below 25 e^- in the full image, in cases needing single photon discrimination at around 250 eV in conjunction with dynamic range adjustment up to $\approx$3 Me^-, and in cases requiring frame rates much higher than 83 Hz.

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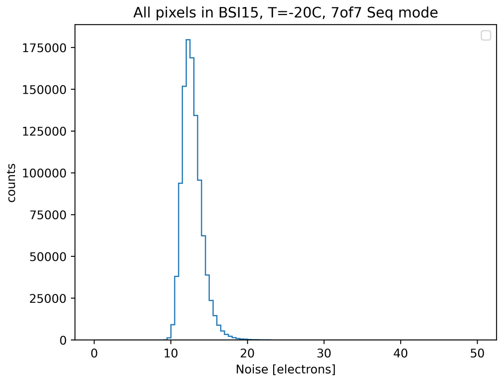

Figure 4: Noise spectrum of all pixels (in the functioning half) of a BSI respin chip measured at $-20\,^{\circ}$C.

There are plans for further improvements in operation and readout system. For operation of the chip, we plan to increase the frame rate up to 300 Hz (for the full-frame) and extend the dynamic range by including the highest gain in the adaptive gain. For improving the readout board, we intend to increase the number of DAQ links to enable a faster acquisition and use the reference pixel data.

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