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Development of silicon interposers with embedded microchannels and metal re-distribution layer for the integration of hybrid detector systems

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ABSTRACT

One of the important challenges in the current radiation detector applications, as we advance in the further integration of the systems, is the cooling of the detectors. The larger heat densities, combined with the complexity of hybrid detector assemblies, complicate the full integration of the sensors, electronics, and services in the whole system. In order to overcome these difficulties microchannel cooling has been proposed to increase the cooling efficiency, reducing the heat transfer path to the detector volume and therefore increasing the heat removal performance, while improving the integration of the cooling with the detector and front-end electronics hybrid system.

In this work, we present the development and fabrication of silicon interposers with embedded microchannels, which also incorporate a metal re-distribution layer (RDL) to contribute further in the integration of the system. These interposers are proposed for their application both in future high energy physics experiments and for advanced systems in photon science where the thermal, material, and integration requirements are very demanding, therefore they can benefit from these developments.

The microchannels and the metal tracks are created in several fabrication steps which are described. Two methods have been followed to produce these interposers, called "pre-processing" and "post-processing", depending on whether the microchannels are created before or after the metal lines. The multiple analysis techniques used to evaluate the different fabrication methods and to assess the final quality of the interposers are presented and the results discussed. Additional considerations are made on the potential of alternative technologies available to create interposers for further applications. With the advent of the Through Silicon Vias (TSV) technology, the proposed solution would provide further alternatives for the electrical interconnection of the detector/electronics hybrid with the external world, facilitating the signal and power input/output.

1. Introduction and framework

In today's radiation detector systems for experimental physics, it is necessary to cool the sensors to low temperatures, normally in the range of −10 to −40 °C. This is because the leakage current produced in these detectors when reverse biased, grows quadratically with temperature and linearly with radiation [1]. This can create problems such as increased noise, increase in the power needed to bias the detectors, which can prevent them to reach full depletion, efficiency loss, or additional increase in temperature due to the Joule effect, which can result in thermal runaway of the detectors [2].

On the other hand, in most of these experiments, the cooling of the sensors must be performed with fluid systems (or even bi-phase coolants) due to the large volume to be cooled or because of the high heat densities involved, limiting or neglecting the usage of air cooling. The cooling is provided by means of pipe networks that carry the coolant to the detector modules where the sensors are located [3]. The modules are the basic unit of the system, which include the particle sensors, the readout electronics, the input/output elements for data, monitoring and command, the power distribution, and the cooling. Once they reach the modules, the pipes are reduced to the smallest technologically feasible size and connected to the detectors, usually through thermal glues and

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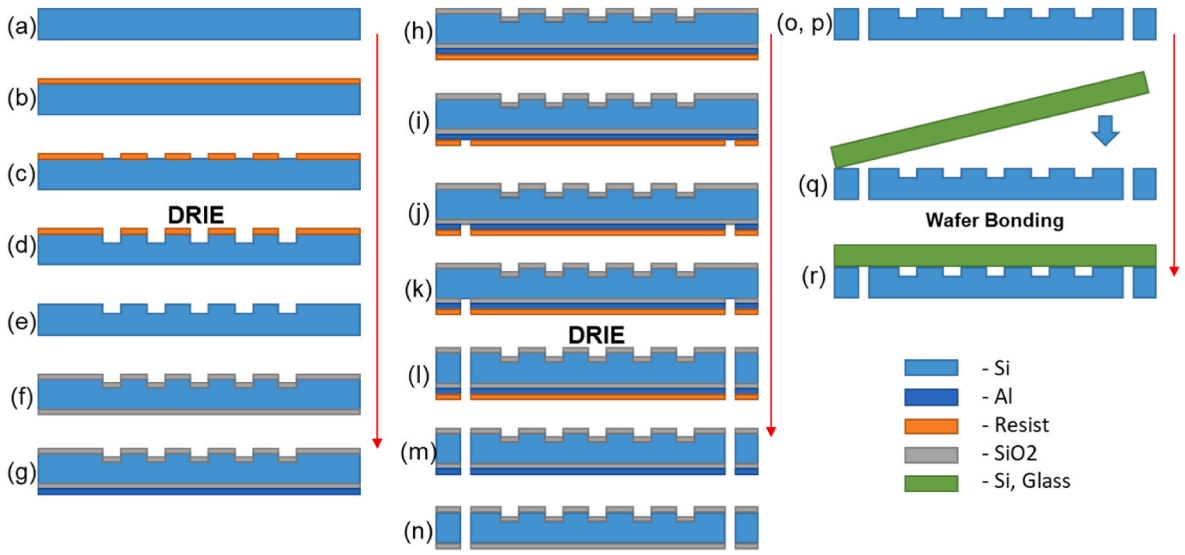

Fig. 1. Schematic view of the technological steps to obtain the embedded microchannels. Indicative letters can be followed in the text.

other thermally conductive elements [4]. The use of such pipes and thermal elements adds complexity to the detector modules and increases the total mass of the system which is a key element in these experiments, since it is necessary to interact as little as possible with the particles to be detected outside of the active sensor area. In addition, the connection of the pipes with the silicon detectors is always problematic due to the fragile and light mechanical elements involved, the complexity of the practical implementation of the assembly, and the thermal resistance of the intermediate elements, which reduces the heat removal efficiency.

In recent years, a new technological proposal for cooling elements with high heat densities has emerged in the field of microelectronics. This is microchannel cooling [5,6]. As electronic devices become smaller and smaller, and integration densities continue to grow at the rate of the famous Moore's Law, the power densities involved in electronic circuits grow enormously, hence it is increasingly difficult to evacuate the entire amount of heat generated in these small volumes. This is how the possibility of evacuating the heat also with high cooling densities and therefore high density "pipes" integrated in the silicon itself, i.e. integrated microchannels, was born [7]. In this way, on the one hand, the cooling power is very high in a small volume, and in addition the thermal resistances are also small, because the microchannels are integrated in the silicon block itself or in intimate contact with the active elements as silicon interposers.

In this work we present the technological developments to further explore this technology by adding interconnection functionality to the cooling interposer with embedded microchannels. The developed interposers provide mechanical support and high-efficient cooling together with a metal layer that facilitates the interconnection of the detector assembly – composed of the sensor plus the front-end electronics – with the back-end electronics and rest of the detector system. In the past we already developed a technology of embedded microchannels on silicon substrates by the use of Deep Reactive Ion Etching (DRIE) and wafer bonding techniques and demonstrated the successful flow and cooling performance [8,9]. Now, we present the extension of this technology to incorporate a metal re-distribution layer (RDL) in order to facilitate the interconnection of the signal and power with the backend electronics.

2. Silicon interposer technology

Fig. 1 shows a schematic view of the fabrication steps to obtain the embedded microchannels. The first column on the left represents the realization of the microchannels in the first DRIE process. We start with a 300- or 500-μm thick double-side polished silicon wafer (a). First, a photolithographic process is done to define the areas where the silicon will be etched to create the deep channels. The mask is designed with a specific edge ring in order to have a better alignment of the channels within the wafer. A special thick resist (6 μm) is used in order to stand the aggressive etching process (b). Once the resist is developed (c), the deep anisotropic etching of the silicon substrate is started. The process is realized in two steps. First, a few microns (~10 μm) are etched deep into the silicon in order to create the alignment marks for subsequent layers. Then, the alignment marks are manually covered with additional resist in order to protect that part of the wafer from the deep etching which could create processing problems later. When the alignment marks are properly covered, the DRIE process continues, this time etching only the area of the microchannels (d). The method employed is the "standard Bosch process" [10] by which two cycles of etching (with SF_6) and passivation (with C_4F_8) are alternated in order to etch the silicon very anisotropically in the vertical direction. In this way, we proceed to

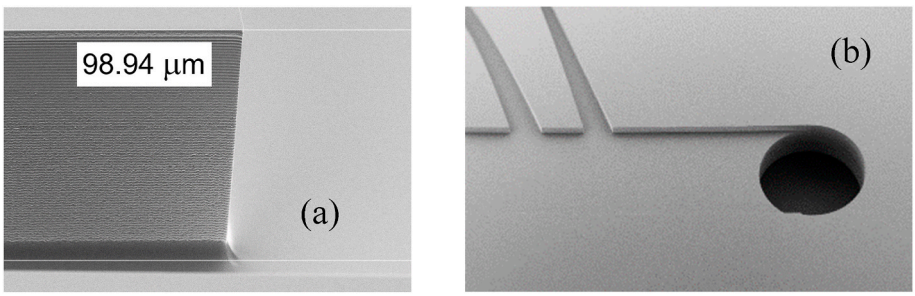

Fig. 2. SEM images of (a) a wall of the microchannels, (b) the inlet/outlet created.

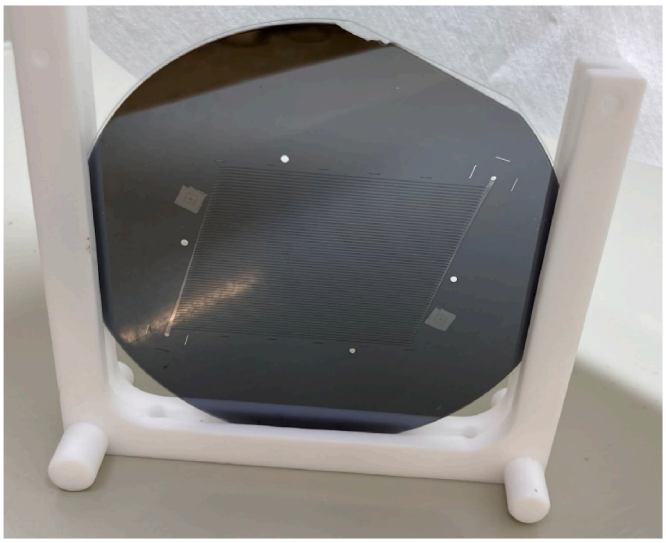

Fig. 3. Anodic bonding assembly of a silicon wafer with microchannels and inlet/outlet through-holes with a glass wafer.

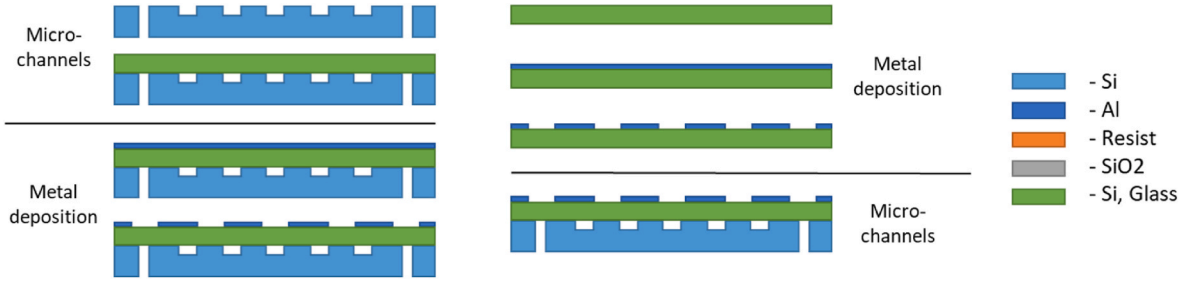

Fig. 4. Schematic view of the technological "pre-processing" (left) and "post-processing" (right) steps to obtain an interposer with embedded microchannels and RDL.

obtain the vertical microchannels to a depth of 100 µm. The widths of the channels that we usually create are in the order to 50–100 µm, although narrower and/or deeper channels could be obtained. The rest of resist can now be removed (e). An example scanning electron microscopy (SEM) image of a microchannel created with this process can be seen in Fig. 2(a) where the typical scalloping produced by the Bosch process in the walls of the microchannels can be clearly seen.

Once the microchannels are created in the silicon substrate, we proceed with the creation of the inlet and outlet. For this we will make the second DRIE process, this time to create a through hole in the substrate. First, we protect both sides of the substrate with the growth of a wet oxide, 500 nm thick (f). Then, we deposit by sputtering in the back side of the substrate (the opposite side to the microchannels) a 1-µm thick aluminum layer (g). This layer will be used to protect the silicon substrate during the long DRIE process. The second photolithographic process is now performed to define the areas where the inlet an outlet will be placed. Then, we precisely align the through holes with the microchannels, using the previously defined alignment marks and a double-side alignment optics. This time a more standard resist is used (2 µm) as it will not be used as a mask during the DRIE process (h). After the development of the resist (i), two etching processes are done. First, the aluminum is removed with a wet etching process from the areas where the through holes will be created (j), and later the 500 µm oxide is also removed from those areas with a dry etching process (k). Later, the second DRIE process is executed to create the through holes (l). The etching is done in two steps, as described above, to define alignment marks in the wafer for further processing. For the last few microns a support wafer is used to avoid problems in the chamber due to the full etch through of the wafer. When the DRIE process is finished, the resist can be removed (m) and the remaining aluminum (n) and oxide (o) are removed by two consecutive wet etching processes. An RCA cleaning process (SC1 H2O:H2O2:NH4OH (5:1:1) at 70 °C and SC2 H2O:H2O2:HCl (6:1:1) at 70 °C) is performed to remove all possible rests of organic or metallic components, and any remaining particles (p). The silicon substrate is now ready for the next steps with the microchannels and the inlet/outlet already defined. A SEM image of an area with the microchannels and inlet/outlet can be seen in Fig. 2 (b).

Once the microchannels and the inlet and outlet are created, we proceed to bury them in a substrate by means of wafer bonding. We have the possibility to do anodic bonding (Si-Glass), eutectic bonding (with an intermediate Si/Au layer), and fusion or direct bonding (Si–Si). At this moment, the optimal process for our purposes is anodic bonding with borosilicate glass wafers because it is a simpler process where we obtain a high yield and for which we have developed a lower temperature processing (350 °C). We use 500 µm thick Borosilicate glass[1] wafers or 300 µm thick MEMpax[2] wafers. For the anodic bonding, both wafers are first cleaned carefully to avoid the presence of any particles or contaminants that could prevent or reduce the quality of the bonding. The silicon wafer is cleaned by a piranha mixture (H2SO4:H2O2 (1:2)) and the glass wafer by an RCA cleaning process. Then the two wafers are aligned and put together in contact and placed into the bonding chamber within the electrodes (q). The parameters we use are.

- Vacuum: 3×10^{-3} mBar
- Temperature: 350 °C
- Pressure: 150 mBar
- Voltage: 1000 V
- Full processing time: 1h 20 m

The result of a fully bonded assembly with microchannels (r) can be seen in Fig. 3.

At this point, we will describe the processing steps to create the metal RDL together with the embedded microchannels. We have investigated two possibilities: One is what we call "pre-processing", by which the anodic bonding is performed *before* the metal layer is deposited and structured; the other option is "post-processing", by which the anodic bonding is performed *after* the metal layer is deposited and structured on the glass wafer. A schematic view of both processes can be seen in Fig. 4. Now we will describe the process of creation of the RDL independently of whether the pre-processing or post-processing option is performed.

The metal layer we use is an alloy of Al(99.5%)/Cu(0.5%) with a thickness of 1 µm. The presence of Cu helps to prevent electromigration in the metal tracks [11]. High-purity grade metal targets are used and deposited by sputtering technique. In the sputtering process the metal atoms are extracted from a target by means of bombardment with Argon ions accelerated in an electric field in a plasma atmosphere. In this way,

[1] Präzisions Glass & Optik Gmbh https://www.pgo-online.com/de.
[2] https://www.schott.com/en-no/products/mempax-p1000322.

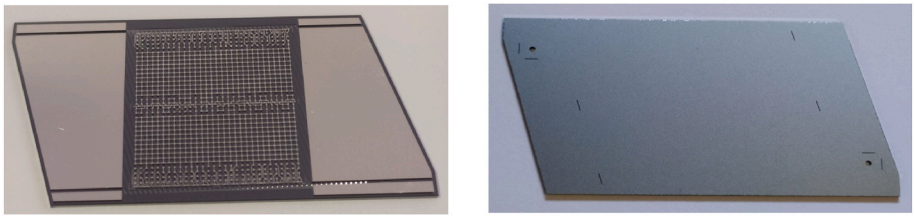

Fig. 5. Front (left) and back (right) side of an interposed fabricated including embedded microchannels and RDL.

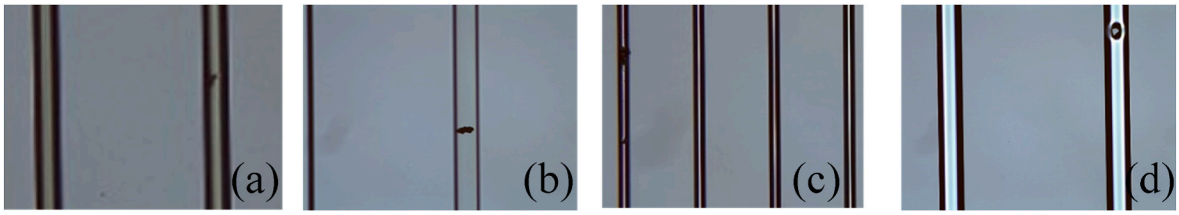

Fig. 6. The different types of defects encountered in the yield investigation of the microchannels.

the aluminum atoms are ejected from the target and reach the substrate with a kinetic energy which favors the metal adherence to the surface, which significantly increases bondability with respect to evaporation deposition techniques [12]. We use a magnetron sputtering process also which improves the efficiency of the deposition and increases the deposition rates [13].

An antireflective positive photoresist is spin deposited on top of the metal to a characteristic thickness of 1.7 m. This resist is then exposed to g-line (436 nm) UV light through a previously fabricated mask containing the layout of the RDL. Only the areas of the resist on top of undesired parts of metal are exposed to UV light. Later, a resist developer, is applied to remove from the surface the areas of the photoresist that have been exposed to UV light. The metal layer is then etched using a chemical wet etching process which only affects the areas not protected by the photolithographic resist, defining the tracks and bonding pads of the RDL. The metal is not etched in the peripheral interposer areas where it is not necessary to remove it in order to assure an optimal etching process. This is followed by a thorough cleaning in deionized water. Next, the remaining resist is removed from the top of the metal motives using a photoresist stripper, leaving the bare metal tracks defined on the substrate. After the full processing of the wafer bonded assembly including the metal RDL layer has been finished, the wafer is cut to the required size of the interposer. We use a diamond blade microelectronic wafer dicer to dice the assembly to the required interposer size. In Fig. 5 we can see picture of the front and back sides of an interposed fabricated with the method described above.

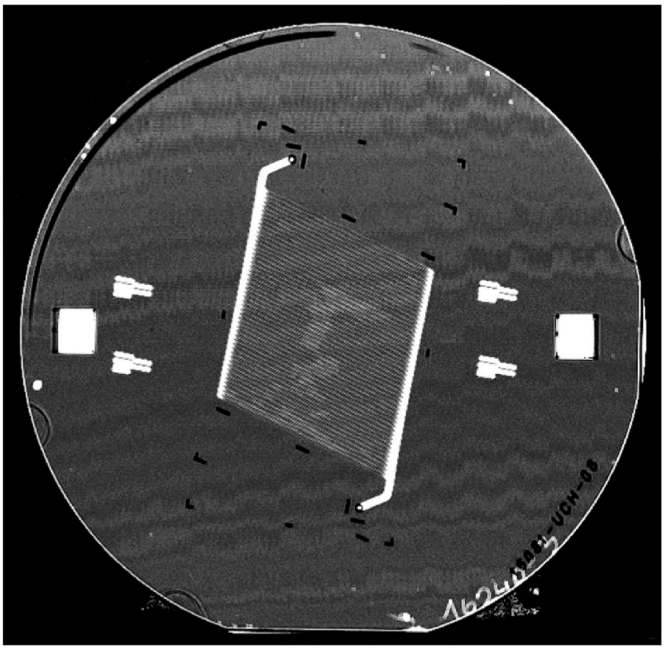

Fig. 7. Scanning Acoustic Microscopy (SAM) image of an anodic bonding assembly.

3. Test results

Several tests have been performed to check the quality of the different processes involved in the fabrication of the interposers. This is a description of the most relevant. Before entering in that it is worth mentioning that in the past, we have already performed fluidic tests of the embedded microchannels fabricated with this technology, with very good results [8,9].

3.1. Microchannel fabrication – DRIE

With respect to the microchannel processing, and the quality of the DRIE processes we do detailed analysis of the structures created, their dimensions and characteristics, by SEM imaging as can be seen as an example in Fig. 2. Additionally, we have conducted an investigation on the yield of the channels created by optical microscopy. Ten wafers processed with the technology described above have been evaluated in detail under the microscope in search for defects in the channels. This represents a sample of 490 channels in total. Fig. 6 shows examples of the different types of defects encountered in the study. On one hand, we have seen minor defects or dust in several channels (Fig. 6 (a) and (b)), which are not problematic as can be removed by a simple air or deionized water flow. Secondly, we have seen three channels with some blocking debris (Fig. 6 (c)). These can be cleaned with additional cleaning process. Finally, we have identified seven channels with "Columnar" channel-etch defects (Fig. 6 (d)). These defects are not blocking the whole channel and would most likely be removed with the first liquid flow in the channels. In any case, these could be a bit more problematic so we consider that we have about a 98.5% yield of good channels. On the other hand, we believe we can improve the process, and avoid most of the defects described above, by using a layer of SiO_2 as a mask for the etching of the microchannels instead of resist.

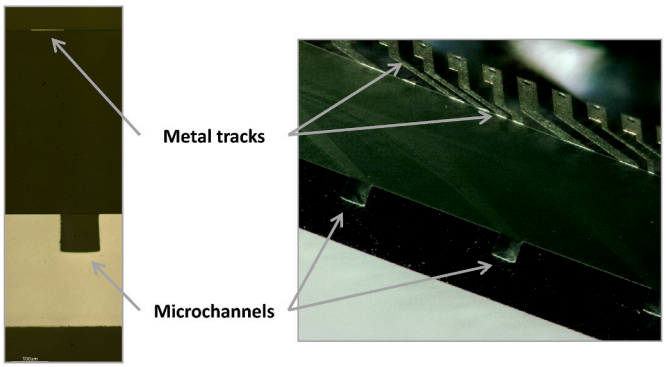

Fig. 8. Cross section of an anodic bonded assembly with embedded microchannels and metal tracks of the RDL.

3.2. Embedded microchannels – wafer bonding

In order to study the quality of the anodic bonding process we use Scanning Acoustic Microscopy (SAM). By this method, voids in the interface between the two wafers bonded can be identified. Fig. 7 shows a typical SAM image of an anodic bonded assembly where only the features specifically designed can be identified, and no additional voids can be seen (except for the very edge where it is not damaging), revealing a good quality of the wafer bonding.

Another method by which we evaluate the bonding quality is by obtaining cross sections of the bonded pieces by reverse engineering methods. Fig. 8 shows two examples of cross sections of interposers where the embedded microchannels can be seen together with the metal tracks of the RDL.

3.3. RDL – metal deposition

We have used several methods to evaluate the quality of the metal deposited, to act as a re-distribution layer (RDL), on the interposers. There are basically two features that are key elements of this metal [14]. On one hand, as this metal will be used as a distribution layer for the power and signals coming from the detector assembly, an important figure-of-merit is the resistivity of the metal itself. On the other hand, the bondability of the metal layer is the other important figure-of-merit, because the interposer will be used for the interconnection between the detector assembly and the backend electronics by means of wire-bonding.

Therefore, we first evaluate the sheet resistance of the deposited metal. We have used two methods: On one hand, we use a four-point-probe resistivity measurement in order to obtain the sheet resistance directly on the deposited metal layer. With this method, we have measured the sheet resistance in 8 positions uniformly distributed across the wafer for several assemblies. The sheet resistance values obtained for three different wafer assemblies with 1 μm thick Aluminum layer are: 33.1 ± 1 mΩ/□, 42.3 ± 4 mΩ/□, and 42.3 ± 5 mΩ/□. These values are compatible with the use of the metal for interconnection purposes. The relative differences between some assemblies and the others are more related to the precision of the measurement itself, with values in the order of mOhms, than with actual technological differences among them.

On the other hand, we have designed Cross-bridge resistors (CBR) test structures [15] to be fabricated on the wafer, together with the RDL. The sheet resistance of the metal tracks can be obtained by electrical measurements performed in a probe station on the CBR structures after the full fabrication. As an example, the sheet resistance values obtained from the probing of 10 CBR test structures uniformly distributed across the wafer in one specific assembly with 0.5 μm metal layer thickness are 63.0 ± 3 mΩ/□. As it can be seen, the result is compatible with the values obtained with the four-point-probe measurement in a metal thickness that is double than this one.

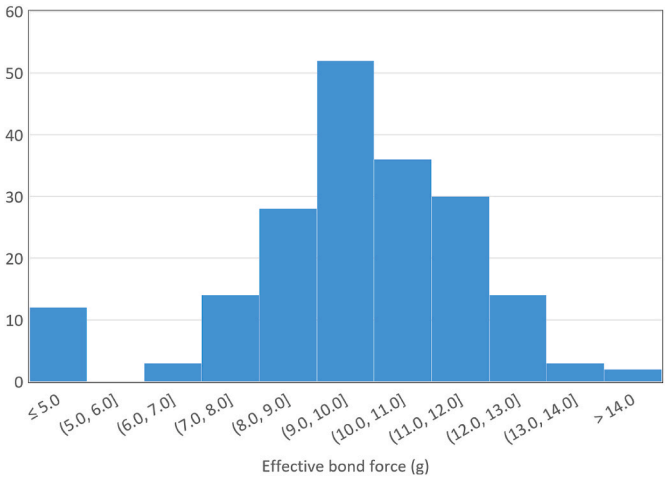

Fig. 9. Bond force distribution obtained from pull tests of an assembly fabricated by the pre-processing method.

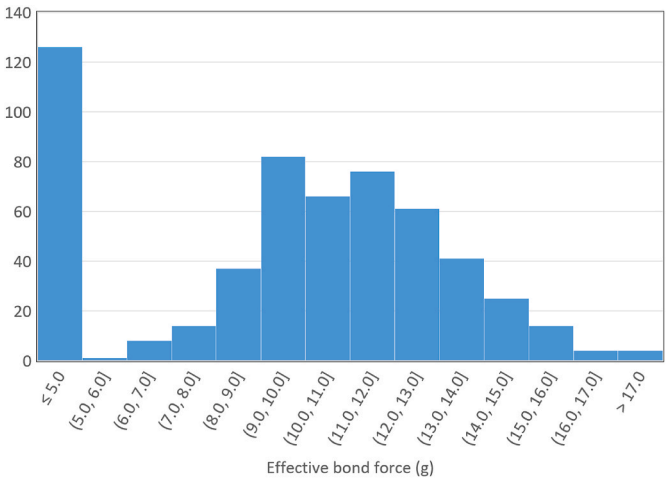

Fig. 10. Bond force distribution obtained from pull tests of an assembly fabricated by the post-processing method.

Finally, the second feature that we have evaluated in the RDL is the bondability of the metal layer. We have performed bonding and pull tests on the deposited metal layers on full assemblies after the anodic wafer bonding process. Here we can distinguish between the cases of pre-processing and post-processing, as explained in section 2. In the pre-processing case, the results are very good, both for the general bondability of the samples, understood as the easiness or difficulty to perform wire-bonds, and the bond force measured in pull tests. We have performed hundreds of wire-bonds, using standard 25 μm aluminum wire, and pull tests of these wires, measuring the force at which the bond is broken. The results of these tests can be seen in Fig. 9. The average force obtained is 9.5 ± 1.3 g. The values below 5 g actually correspond to failed initial bonds, therefore they have not been included in the statistics.

In the post-processing case, we have had come cases of bad adherence of the metal to the substrate which resulted in bad metal bondability. We have attributed this to the effects produced by the anodic bonding on the deposited metal. The relatively high temperature of the anodic bonding process, plus the pressure applied to the metal during that step, creates stresses in the metal which produce bubbles and a reduction of the adherence of the layer to the surface. In order to avoid this problem, we made the sputtering deposition of the metal at high

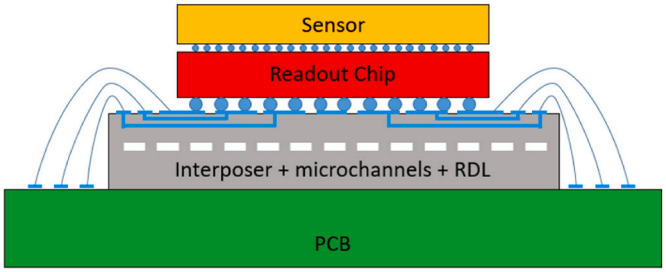

Fig. 11. Depiction of the application scheme of the interposers presented here for a generic hybrid detector system. A similar scheme could be applied for a monolithic sensor configuration.

temperature (350 °C) corresponding to the temperature used in the anodic process. In this case, the metal layer is actually relaxed during the anodic process and the metal adherence is not degraded.

Wire-bonding and pull tests have been performed also on assemblies made with the post-processing method with satisfactory results as can be seen in Fig. 10. The average force obtained is 11.2 ± 2.6 g. It can be seen that there is a larger number of very low values in the plot which correspond to initial bonding failures (and not included in the statistics). This can be related to dirt in the electrodes and also to ion displacement within the glass wafer inherent to the anodic bonding process. These factors create punctual defects in the metal. We are investigating this further.

3.4. Conclusion and future work

We have presented the technology developed to create silicon interposers with embedded microchannels and redistribution layer (RDL). The basic technology of the embedded microchannel was presented in the past and their functionality, both with fluidic and thermal tests already demonstrated. The detailed fabrication process to obtain the interposers has been presented here, and the several measurement methods to evaluate the quality of the different technological steps have been described. The results of these tests are successful and the fists interposers have been fabricated. The technology is ready for demonstration in actual prototype systems.

The next steps in this work are the demonstration in actual prototypes. These interposers are proposed for their application both in future high energy physics experiments and for advanced systems in photon science, where the thermal, material, and integration requirements are very demanding, therefore they can benefit from these developments. Some foreseen applications in future particle physics experiments may have more demanding requirements in terms of material budget, in the order of 0.2%X0, but less demanding in power densities (~100 mW/cm^2), while other applications, as in photon science, might be less demanding in material budget, but highly demanding in heat dissipation, with power densities in the order of a few W/cm^2. A schematic view of the envisioned use of these interposers in a general pixel assembly system is portrayed in Fig. 11.

Future developments will be dedicated to the demonstration of the fluidic and thermal behavior of the interposers in actual prototypes, similar to the scheme shown in Fig. 11. Also, we are planning the exploration of additional technological options for the interposers that could add advantages to the full assembly, like the addition of Through Silicon Vias (TSV) to improve the connectivity of the full system.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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