Prototyping experience with Ge micro-strip sensors for EDXAS experiments

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ABSTRACT

Energy dispersive X-ray spectrometers provide a method for the fast data acquisition of X-ray absorption spectra. The intensity of the spectral components of a polychromatic beam is detected simultaneously after being dispersed in space, and being transmitted by an experimental sample. The cryogenic detector system called XH deploys a germanium micro-strip sensor to perform such measurements. Here, the geometrical position of each strip is correlated to a specific spectral component of the dispersed beam.

The prototyping experience reported in this work is related to the upgrade of the cryostat unit of the XH detector system. This upgrade was carried out in collaboration with beam-line ID24 at the European Synchrotron Radiation Facility (ESRF).

Two 90 mm wafers of p-type high purity germanium were manufactured. Wafers contained test structures and micro-strip sensors made of 1024 strips with 50 μm pitch. Electrical and in-beam tests were performed to verify the performance of this technology. The measurements included capacitance–voltage characteristics; stress-tests like temperature cycling testing and burn-in tests; leakage current as a function of sensor temperature; charge-collection as a function of time; a test-run of a pump and probe experiment.

Results are reported below showing that this sensor technology survived the extensive thermal and electrical stress-tests, and that it was able to measure the physical variations created by a laser shock on a sample of Fe–10%wtNi.

1. Introduction

The deployment of energy dispersive spectrometers in Energy Dispersive X-ray Absorption Spectroscopy (EDXAS) makes possible the fast data acquisition of X-ray absorption spectra [1,2]. In this technique, the experimental sample is irradiated with a polychromatic beam. The beam is focused on the sample and its spectral components are linearly dispersed in angle when moving away from the focal point. The dispersed X-rays transmitted by the sample are then detected with a position sensitive sensor like a Ge micro-strip sensor. The geometrical position of each micro-strip is correlated to a spectral component of the polychromatic beam. The simultaneous detection in each micro-strip of the intensity of the transmitted beam, provides a simultaneous acquisition of the spectral components of an X-ray absorption spectrum.

The fast data acquisition capability provided by the energy dispersive spectrometer is exploited by scientists to perform time resolved experiments [3–6]. Changes in the X-ray absorption spectrum are measured as a function of time to describe chemical and physical

processes in matter [7,8]. Repeated exposures of the sample to X-rays are recorded sequentially by the detector.

Time resolved experiments can be performed also with the pump and probe technique [9,10]. In this case, the sample is probed by the X-rays at a given delay with respect to the excitation stimulus (pump). The measurement can be repeated multiple times on the same sample with non-destructive excitation stimuli. Or it can be repeated by using multiple identical samples where the excitation pulses have destructive effects.

The work presented in this publication focuses on verification tests performed on Ge micro-strip sensors produced by Mirion Technologies in Lingolsheim (FR) [11,12]. This activity was part of the prototyping phase for the upgrade of the cryostat unit of the XH detector system [13–16]. The objective was to enhance the technical maturity of the cryostat unit by improving its thermal performance, and by instrumenting it with commercially available Ge sensors.

The cryostat upgrade was carried out in collaboration with beam-line ID24 [17,18] at the European Synchrotron Radiation Facility
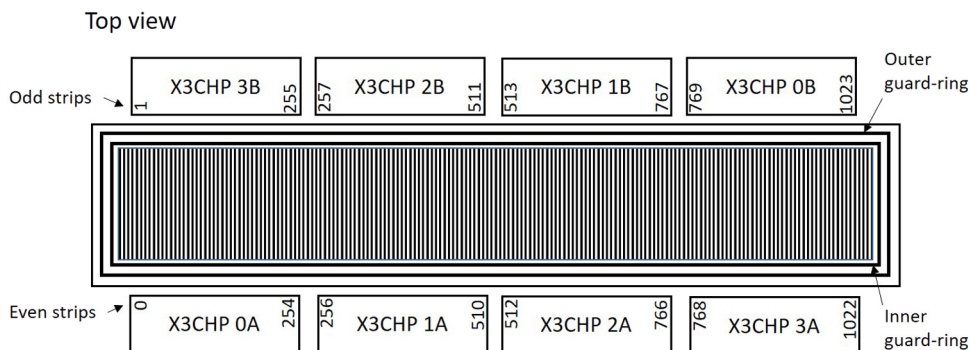
Fig. 1. Sketch of the cryogenic module supporting 1 Ge sensor and 8 X3CHIPs. Even strips are wire-bonded to the 4 X3CHIPs in set A and odd strips to the 4 ASICs in set B.

(ESRF) in Grenoble (FR). The activity was part of the broader beam-line refurbishment connected to the construction of the Extremely Brilliant Source (EBS) [19], a fourth generation synchrotron. ID24 scaled up its capabilities by building the High Power Laser Facility (HPLF) [20–22] as part of the refurbishment. In its first stage, the facility couples a 100 J ns-pulse laser to an energy dispersive spectrometer to perform EDXAS experiments in pump and probe mode. The HPLF targets dynamic compression techniques to study extreme conditions of pressure and temperature in matter. A representative case is the study of warm dense matter [9]. This is an exotic state which is relevant to the description of a planet interior in planetary science.

2. Device under test

Ge micro-strip sensors were tested to verify their performance and reliability in EDXAS experiments. This is because a new sensor manufacturer (Mirion Technologies) was selected for this latest upgrade of the cryostat unit of the XH detector system.

The XH is a cryogenic detector system made of two main independent units: a cryostat unit and a data acquisition (DAQ) unit. The cryostat unit encases a cryogenic module supporting one Ge micro-strip sensor and the related front-end electronics (i.e. X3CHIPs). A sketch of the cryogenic module is shown in Fig. 1. A liquid nitrogen filled Dewar is connected via a rod to the cryogenic module to provide cooling. The DAQ unit is electrically connected to the cryostat unit and it is operated in atmosphere. It provides clock and control signals to the front-end electronics, and it receives and processes analogue data.

A total of 8 X3CHIPs are installed in the cryostat and wire-bonded to the sensor strips. The X3CHIP is a charge integrating ASIC designed in AMS 350 nm technology. Each of its 128 front-end channels is made of a pre-amplifier followed by a sample-and-hold circuit. Within an ASIC, channels are read out in groups of 32 by the same multiplexer. This equates to a total of four multiplexer per ASIC. The X3CHIP is capable of integrating a maximum charge of 50 pC per front-end channel. The minimum integration time is nominally 180 ns and the maximum is 1 s. The dead time is 1.2 μs which is dominated by the pre-amplifier reset time.

The Ge sensor is made of 1024 strips with 50 μm pitch. The strip length is 5 mm. It is a back illuminated device. Two guard-rings are surrounding the array of strips as shown in Fig. 1. Wire-bonding pads were placed at the upper-end of odd strips and at the lower-end of even strips. This leads to an alternated wire-bonding pattern where even strips are connected to the 4 X3CHIPs in set A, and odd strips to the 4 ASICs in set B as sketched in Fig. 1.

Two 90 mm wafers of p-type high purity germanium were processed by using a proprietary semiconductor process technology. The photolithographic process is based on a double-sided wafer process. Sensors have strips patterned on the front-side of the wafer, acting as the junction contact. The back-side is a p-type implant acting as an ohmic contact, used to apply a negative bias voltage.
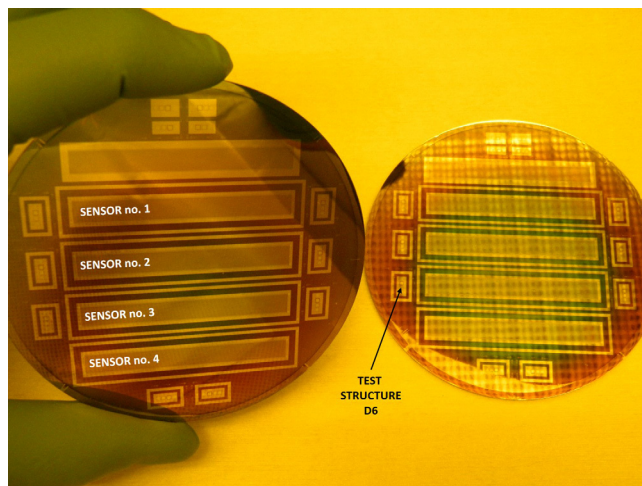

Fig. 2. Two 90 mm wafers of p-type high purity germanium carrying 1 sensor with single guard-ring, 4 sensors with double guard-ring and 8 test structures with double guard-ring.

Wafers are shown in Fig. 2. Each wafer has 4 sensors with 1024 strips on a 50 μm pitch surrounded by a double guard-ring. A total of 8 test structures with double guard-ring were processed on the wafer. They were used to perform quality assurance tests like capacitance–voltage measurements. One sensor with a single guard-ring was included in the wafer layout, but it was not used in this work.

The wafer thickness was selected to be 1.5 mm. This thickness is sufficient to fully absorb X-rays up to 30 keV and nearly up to 40 keV. In fact, ~1% of X-rays are escaping at 40 keV when using a 1.5 mm thick bulk [23]. The energy range of interest for applications at ID24 is 5–27 keV.

3. Tests overview

Measurements on test structures and micro-strip sensors were performed to verify the performance of Ge sensors. They include electrical and in-beam tests.

The test structures were used to assess the depletion voltage of the devices by measuring capacitance–voltage (CV) characteristics.

Two micro-strip sensors were installed into two fully instrumented prototype cryostats. The two prototype cryostats were mechanically identical. They did not reach a target temperature on the sensor of ~−170 °C at ~11.5 W. They were deployed to enable sensor testing while a production version of the cryostat was being developed. One unit was used to stress-test the sensor, electronics, interconnection and mechanics by temperature cycling testing. Current–voltage (IV) characteristics were measured at each temperature cycle and compared.

This unit was also used to measure the correlation between leakage current and temperature at different voltages.

A second cryostat unit was used to study charge-collection in the sensor as a function of time for different parameters like bias voltage and X-ray flux. For this purpose the unit was in-beam tested at ID24 including a test-run of time resolved experiments performed with the pump and probe technique.

Experimental procedures and results are described for the different tests in the following sections.

4. Electrical tests

4.1. CV characteristics on test structures

Capacitance as a function of bias voltage was measured on test structures after sawing the wafers. These measurements were used to estimate the depletion voltage of the 1.5 mm thick wafer.

The details of a test structure are shown in Fig. 3(a). Here, four different pads with 1 mm^2 area are visible. They are surrounded by a double guard-ring structure. The pad under test is representative of the layout of the Ge micro-strip sensors. This pad has a 25 μm gap from the inner guard-ring.

During the measurement, the positive bias voltage was applied to the pad under test. Both guard-rings, all the other pads and the back contact were connected to ground. The frequency used to measure the capacitance was 1 MHz. The voltage was swept from 0 V to 200 V in steps of 10 V.

Curves are presented in Fig. 3(b) at two different temperatures for a representative test structure. This was structure D6 on wafer 2 as numbered in Fig. 2. All the curves plateau at ~25 V. This is because the depletion region reached the back plane of the sensor. The capacitance per unit area is approximated to ~1 pF/mm^2.

### 4.2. Temperature cycling testing

A micro-strip sensor was wire-bonded to the X3CHIPs and installed into a prototype cryostat. This was sensor 1 from wafer 1 as numbered in Fig. 2. Unfortunately, during the wire-bonding operation one X3CHIP got permanently damaged. This was ASIC 3B as numbered in Fig. 1.

Despite this inconvenience, the cryostat unit was deemed suitable to perform stress-tests on sensor, electronics, interconnection and cryostat mechanics. These tests consisted of temperature cycling the cryostat 105 times and monitoring its performance at each iteration. The temperature cycling tests were conducted to determine the ability of components and solder interconnects to withstand mechanical stresses induced by alternating high and low temperature extremes. Permanent changes in electrical and/or physical characteristics can result from these physical stresses.

A temperature cycle generally required ~48 h to complete. It started by pouring liquid nitrogen (LN2) into the cryogenic Dewar. It ended when all the LN2 in the cryogenic Dewar boiled off and the internal components of the cryostat reached room temperature. On average, a temperature cycle spanned a ΔT on the sensor of ~193 °C, typically from ~+20 °C down to ~−173 °C. The maximum ΔT achieved on the sensor was ~228 °C, from ~+55 °C down to ~−173 °C.

The data taking of the 105 temperature cycles was carried out over two sessions. The first session ranged from temperature cycle 0 to 49. The second session progressed from temperature cycle 50 to 104. Each session required about six months to complete.

The outer guard-ring of the sensor was set to floating all the time during the data taking. The inner guard-ring was set to ground for those tests where the ASICs were power off, like the IV tests. The inner guard-ring was set to a reference voltage of ~0.9 V for those tests where the X3CHIPs were powered on, like the pedestal measurements. In this case, the reference voltage of the pre-amplifiers in the X3CHIPs, connected to each strip was set ~0.9 V.
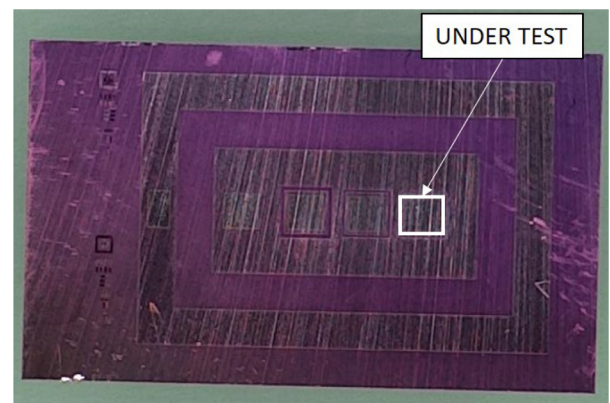
(a)
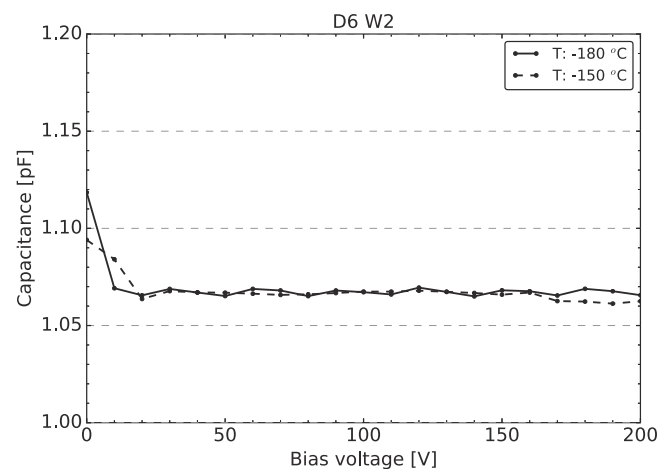
(b)

Fig. 3. (a) Test structure used in CV measurements. The pad under test has a distance from the inner guard equal to that used in the micro-strip sensor layout (25 μm). (b) Capacitance as a function of voltage for a representative test structure at two different temperatures: −180 °C, −150 °C.

The cryostat unit was vacuum-pumped periodically. The temperature and time duration of the vacuum-pumping operation were not kept constant. Fig. 4(a) details in its textbox the duration and temperature of each bake-out. In addition, Fig. 4(a) shows the break down of the number of temperature cycles performed after each bake-out. In this figure, the term bake-out is used to describe all the vacuum-pumping cycles, at any temperature. This includes bake-out 0 where the cryostat unit was simply vacuum-pumped for about seven days at room temperature (i.e. without applying additional heat). The longest and hottest bake-out had a temperature on the sensor of ~+55 °C for a period of ~4 days.

The cryostat was not vacuum-pumped after each temperature cycle because this operation would have substantially increased the time necessary to acquire a sample of about 100 temperature cycles. Instead, it was decided that a periodic bake-out of the system was a quicker and a preferable course of action for a stress-test. By doing so, the sensor was contaminated by out gassing processes inside the cryostat in between bake-outs, affecting its surface current. Additionally, the system was exposed to a higher thermal excursion after each bake-out. Both factors adding stress to the sensor.

4.2.1. Cool-down stability

The temperature variation on the sensor is shown in Fig. 4(b) for the first ~2.5 h of cool-down . These curves were used as a proxy to

judge the mechanical stability of the cryostat over multiple temperature cycles. Fig. 4(b) shows the temperature variation on the sensor for 103 out of the 105 thermal cycles. This is because two cool-down profiles were lost during data taking because of network problems which affected the DAQ operation. It is possible to see that all profiles have a good overlap. The average temperature measured after one hour of data logging is ~-138 °C with a standard deviation of 0.7 °C. After two hours of data logging, the average temperature is ~-156 °C with a standard deviation of 0.5 °C. The small values of the standard deviation support the fact that the cryostat mechanics and the assembly are not showing any noticeable change in performance, due to mechanical relaxation after repeated temperature cycling.

The initial temperature of the cool-down profile varies from room temperature to $\sim+55$ °C. This is because the cryostat and the sensor were periodically subject to bake-out operations as mentioned above.

4.2.2. Electronic pedestals stability

The first set of electrical tests within a temperature cycle aimed at checking that sensor, electronics and interconnection did not show permanent changes in electrical performance because of the mechanical stress induced by alternating high and low temperature extremes. For this purpose, electronics pedestals of the first (no. 0) and the last (no. 104) temperature cycle are presented in Fig. 5. The comparison is in ADU values of dark current integrated for 1 ms using a feedback capacitor of 10 pF and applying a bias voltage of -150 V on the sensor. Both measurements were taken at a temperature of ~-159 °C. Note that the comparison is only focusing on strips 256 to 1023. In fact, strips 0 to 255 were rejected because they are in the region which is connected with an interleaved pattern to the broken ASIC 3B (see Fig. 1).

Fig. 5 shows two clusters of defective strips: strip 436, and strips 867–874. Strip 867 and 874 show lower pedestal values at temperature cycle 104 with respect to temperature cycle 0. Except for this change around a defective cluster, the two curves overlap well. This supports the fact that sensor, electronics and interconnection were able to withstand repeated temperature cycling without showing a substantial change in their electrical properties.

4.2.3. IV curves stability

The last stage of electrical testing within a temperature cycle consisted of performing sequentially 5 IVs on the sensor. In a production systems, the target temperature for the sensor operation is ~-170 °C at ~11.5 W. By using a prototype cryostat, temperatures ~-170 °C could only be achieved by powering off the X3CHIPs. In this way, the sensor temperature was regulated at ~-173 °C by using heater resistors mounted on the carrier boards of the X3CHIPs.

Each IV curve was measured by scanning the bias voltage from 0 V to -175 V, in steps of 1.25 V. Fig. 6(a) shows the comparison of two sets of IVs acquired in the first (no. 0) and last (no. 104) temperature cycle. The two sets of IVs have a similar trend and similar values. The last set of IVs is showing a lower current because the sensor had a bake-out at $\sim+55$ °C for about 4 days. For the first set of IVs, the cryostat was vacuum-pumped at room temperature for about a week. The cryostat unit and the sensor are cleaner in last temperature cycle with respect to the first one. This results in a reduced surface current on the sensor.

The first IV of the set in the first (no. 0) temperature cycle is showing some instability which is possibly due to micro discharges in the sensor.

The heat map presented in Fig. 6(b) shows all the 525 IV curves performed over the 105 temperature cycles. The current limit was set to -25 μA except for the first three temperature cycles. The sensor leakage current shows a broad spread of values for bias voltages higher than -90 V. The spread is ascribed to an increase in surface current triggered by an accumulation of contaminants on the sensor surface. A bake-out cycle was performed periodically to remove contaminants and to recondition the leakage current. A temperature of $\sim+55$ °C applied on the sensor for a minimum time of ~50 h was identified as the optimal procedure. The sensor is much less sensitive to surface contaminations for bias voltages lower than -90 V.
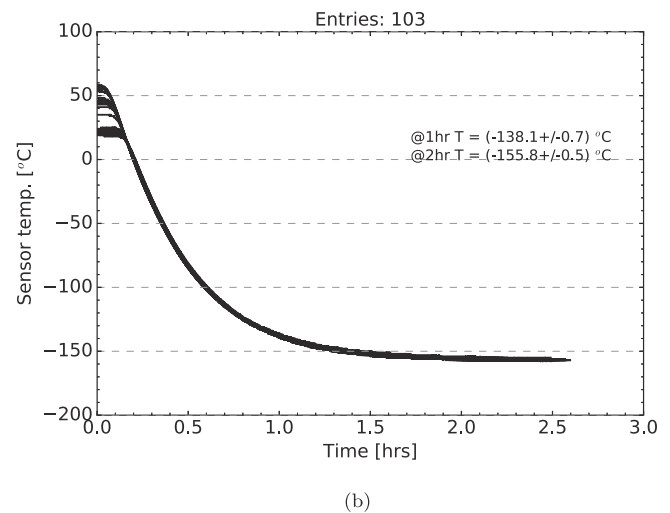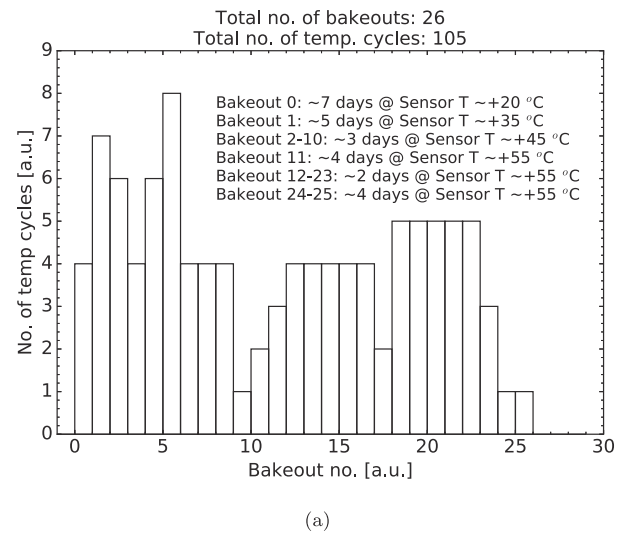

(a)

(b)

Fig. 4. (a) Number of temperature cycles performed after each bake-out operation. The temperature and time duration of each bake-out is reported in the textbox. (b) Cool-down profile for 103 out of 105 temperature cycles.
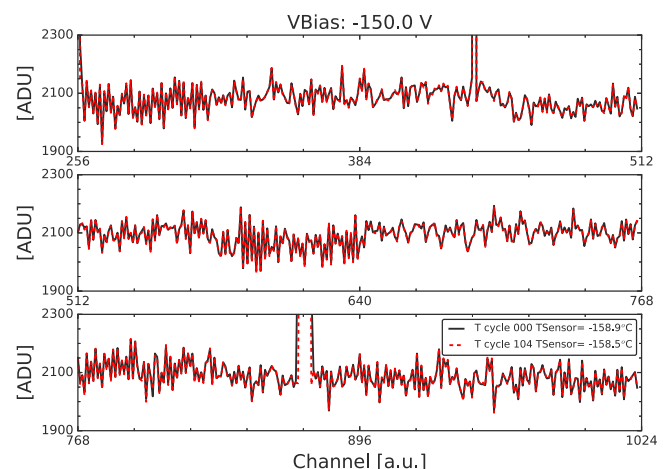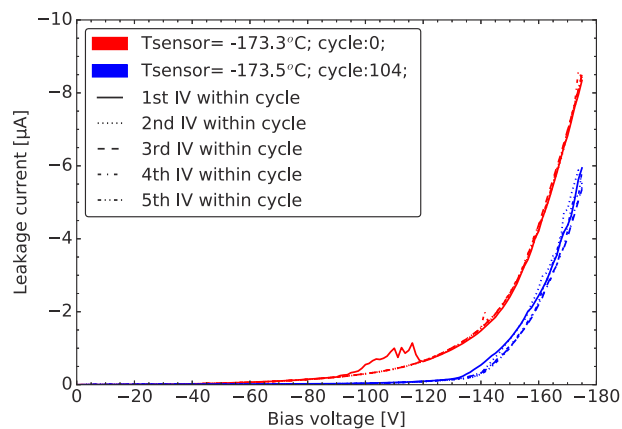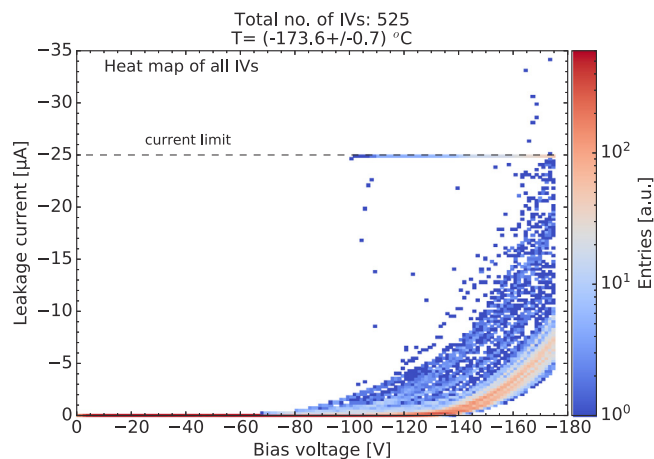

Fig. 5. Pedestals in ADU were compared for the first (no. 0) and last (no. 104) temperature cycle. Apart for a small difference in strip 867 and 874, the overlap is good. This confirms that sensor, electronics and interconnection were able to withstand repeated temperature cycling without showing a substantial change in their electrical properties.

(a)

(b)

Fig. 6. (a) Comparison of two set of IVs acquired in the first (no. 0) and last (no. 104) temperature cycle. (b) Heat map of all the 525 IV curves performed over the 105 temperature cycles.

4.3. Reliability tests post temperature cycling testing

The sensor underwent further tests to validate its reliability after completing the temperature cycling testing.

The first test consisted of monitoring the total leakage current of the sensor and its temperature for 21 days. The graph is presented in Fig. 7. The bias voltage on the sensor was set to −175 V and the sensor temperature was ∼−174 °C. It is observed that the leakage current showed higher fluctuations in the first ∼5 h of data taking. And that after ∼7 days, the leakage current settled to ∼6.0 μA. No evidence of run-away in the leakage current was observed during this period. The cryostat unit was baked-out for ∼4 days at ∼+55 °C before performing this measurement. The outer guard-ring of the sensor was set to floating and the inner guard-ring was set to ground. The ASICs were powered off.

The second measurement which was performed on the sensor consisted of repeating 50 IVs at a higher temperature of ∼−155 °C. All the IV curves were measured sequentially by scanning the bias voltage from 0 V to −175 V, the voltage step was 1.25 V. Fig. 8 shows that all the 50 IV curves overlap well. Furthermore, the value of the leakage current is compared for each IV iteration at three selected bias voltages: −95 V, −135 V, −175 V. At a higher bias voltage of −175 V, the leakage current is fluctuating slightly more than at the other settings. The cryostat unit was baked-out for ∼2 days at ∼+55 °C before performing this measurement.

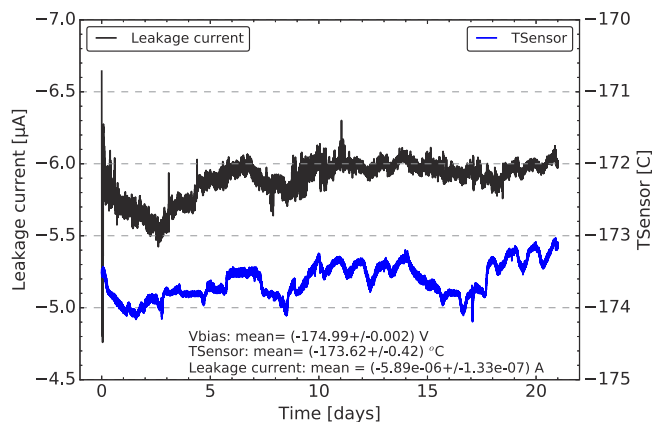**Fig. 7.** Total leakage current of the sensor and its temperature monitored for ∼21 days.

The outer guard-ring of the sensor was set to floating and the inner guard-ring was set to a reference voltage of ∼0.89 V. The X3CHIPs were powered on and the reference voltage of the pre-amplifiers connected to each strip was set to ∼0.89 V.

The ASICs were switched on in this data taking because of the higher temperature. This enabled the quantification of the leakage current in a single strip via the X3CHIPs. The leakage current in each strip was calculated by finding the difference between the dark-current offsets for two integration times, then dividing this difference by the Δt of the two integration times. For the results presented here, the longest integration time was set to 10 ms and the shortest integration time was 1 ms. Therefore, the difference between the dark-current offsets of the long and the short integration times was divided by 9 ms in order to calculate the strips leakage current.

The average leakage current of a strip as a function of bias voltage is shown in Fig. 9(a) for all the 50 iterations. It is observed that the leakage current decreases at higher bias voltages and that it plateaus for values greater than the depletion voltage (∼−25 V). All the curves are superimposed well. A detailed testing to understand this trend has not been performed at this time. Nonetheless, a more in depth analysis on the existing dataset hints towards the fact that the current in a strip is affected by mismatches of reference voltage between strips, and between strips and inner guard-ring. These mismatches are of the order of ∼1 mV or less, and they can produce a strip to strip current and a strip to inner guard-ring current. It is not possible to measure the current flowing in the inner guard-ring with the XH system. The amplitude of these electric currents seem also dependent on the amount of free charge carriers in the bulk.

In Fig. 9(b), the value of the average dark current in a strip was plotted for each IV iteration for three selected bias voltages: −95 V, −135 V, −175 V. The three curves have a steady and comparable trend.

The average value of leakage current in a strip as presented above was calculated by selecting a sample of 750 strips, out of 1024. Strips 0–255 were rejected because they are part of the area connected in interleaved mode to broken ASIC 3B. Strips 436 and 867–874 were defective strips and therefore also discarded. And finally a set of 9 strips spread across the sensor area were also excluded because they had IVs with a trend different from the rest of the population.

4.4. Temperature scan

The temperature on the sensor was scanned from ∼−158 °C to ∼−141 °C with an average step of ∼3.4 °C. The temperature was regulated at each set-point via heather resistors mounted on the electronics boards carrying the X3CHIPs. The X3CHIPs were switched on in this measurement to quantify the dark current in each strip. One IV curve
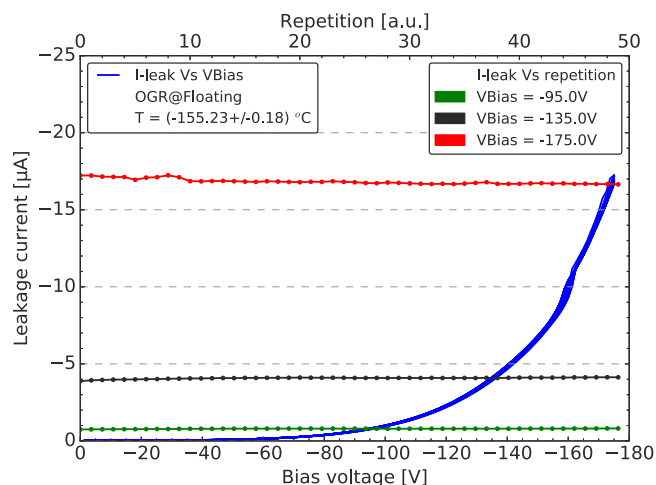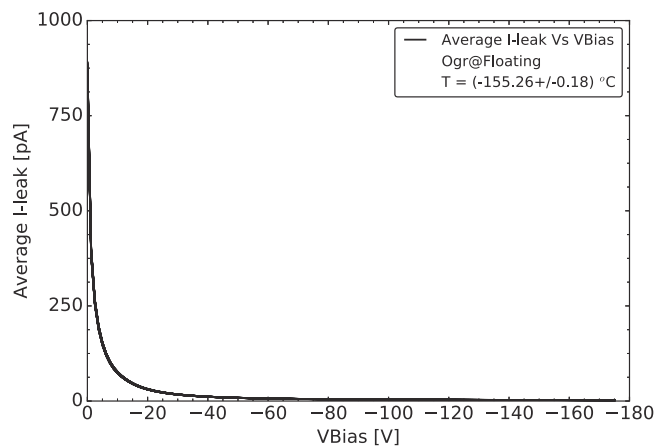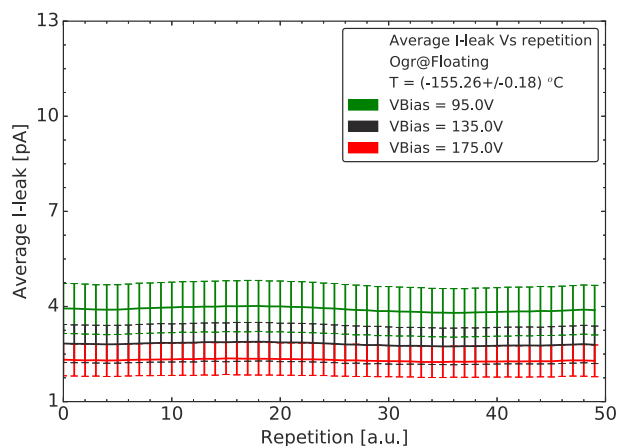
Fig. 8. Sequential measurement of the total leakage current over 50 IVs at a temperature of ∼−155 °C. The total leakage current was also plotted as a function of the IV iteration for three selected bias voltages: −95 V, −135 V, −175 V.

(a)

(b)

Fig. 9. (a) Sequential measurement of the average leakage current of a strip over 50 IVs at a temperature of ∼−155 °C. (b) The average leakage current of a strip was plotted as a function of the IV iteration for three selected bias voltages: −95 V, −135 V, −175 V.

was measured at each temperature by scanning the voltage from 0 to −175 V in steps of 1.25 V.

The outer guard-ring of the sensor was set to floating and the inner guard-ring was set to a reference voltage of ∼0.89 V. In the X3CHIPs, the reference voltage of the pre-amplifiers connected to each strip was set to ∼0.89 V.

Fig. 10(a) presents the dependence of the total leakage current on sensor temperature for four selected voltages: −55 V, −95 V, −135 V and −175 V. The general trend for all the curves is that a lower temperature decreases the total current. Nonetheless the decrease in current has a different magnitude for the different bias voltages. The higher is the bias voltage the higher is the effect of temperature in reducing leakage current. It is observed that the highest leakage current resulting from a bias voltage of −175 V has the strongest dependence on temperature. The behaviour of the total current is a combination of bulk current and surface current. It comprises of current contributions from the double guard-ring region and from all the strips, including defectives strips.

Fig. 10(b) shows the average leakage current in a strip as a function of temperature for the same four voltages. The identical population of 750 strips was used in the calculation as previously described. The trend in all curves shows that a colder sensor has a lower leakage current. This is because a colder sensor has a lower thermal generation of charge carriers. In this case, the temperature scan has a greater effect in reducing the leakage current at lower bias voltages.

5. In-beam tests

A second unit of the prototype cryostat was assembled and in-beam tested at ID24. The data acquisition took place before the long shutdown of the synchrotron for the EBS upgrade. The sensor installed in this cryostat was number 3 from wafer 1 as numbered in Fig. 2. The synchrotron was configured with the fill pattern called 4 bunch. In this configuration, 4 identical bunches of electrons circulated the storage ring generating a maximum current of 40 mA. The spacing between bunches was 700 ns and a single X-ray pulse had a width of ∼100 ps. The 4 bunch mode is the fill pattern which provides the most intense photon flux per electron bunch.

Two types of test were performed. The first one consisted of measuring the time required by the sensor and the X3CHIPs to collect the charge ionised by X-rays in the sensor. The second one consisted of a test-run of a pump and probe experiment. This consisted of setting up and running together the prototype cryostat of the XH system and a prototype of the laser exciting the sample. In both tests, the system was synchronised to the radio-frequency clock of the accelerator (∼352 MHz). A frame rate of 355 kHz was set on the system matching the revolution frequency of the synchrotron. In this way, a single X-ray flash per revolution was captured by the XH system.

### 5.1. Charge-collection as a function of time

Charge-collection as a function of time was studied for individual strips.

Initially, the intensity distribution of the spectral components of a single X-ray pulse hitting the sensor, was examined to select strips with different photon fluxes. The intensity distribution is shown Fig. 11(a). The beam had central energy of ∼7.5 keV. The flux in each strip was approximated to a number of photons by dividing the values of integrated charge in a front-end channel by the central energy of the polychromatic beam: ∼7.5 keV. Pedestal subtraction was performed before estimating the flux. Fig. 11(a) displays the typical intensity distribution of X-rays generated by the undulators at ID24. The peak flux is ∼7500 photons and it decreases to a few 100's of photons.

Fig. 11(a) was used to select five strips with different X-ray flux. The charge-collection profile as a function of time is presented for this set of strips in Fig. 11(b). To reconstruct the charge-collection profile,
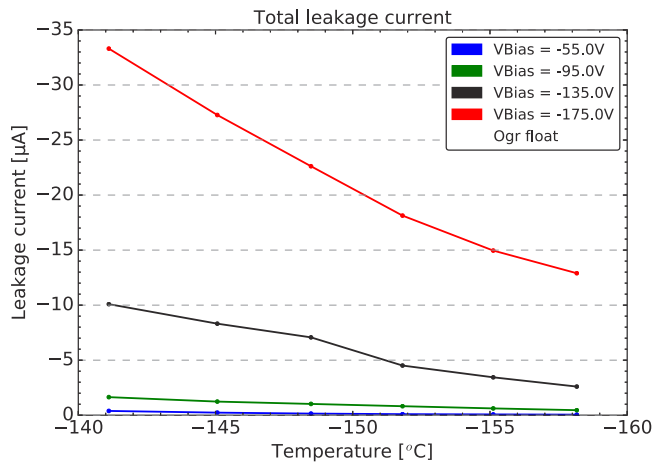
(a)
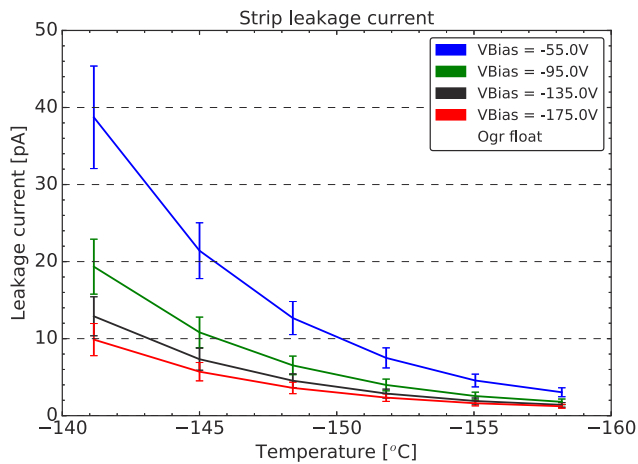
(b)

Fig. 10. Leakage current as a function of temperature: (a) total leakage current; (b) average leakage current of a strip. In both cases, four different voltages were considered: −55 V, −95 V, −135 V, −175 V.

(a)

(b)

Fig. 11. (a) Intensity distribution of the spectral components of a single X-ray pulse of polychromatic beam hitting the sensor. (b) Charge-collection as a function of time for different X-ray intensities, at a constant bias voltage.
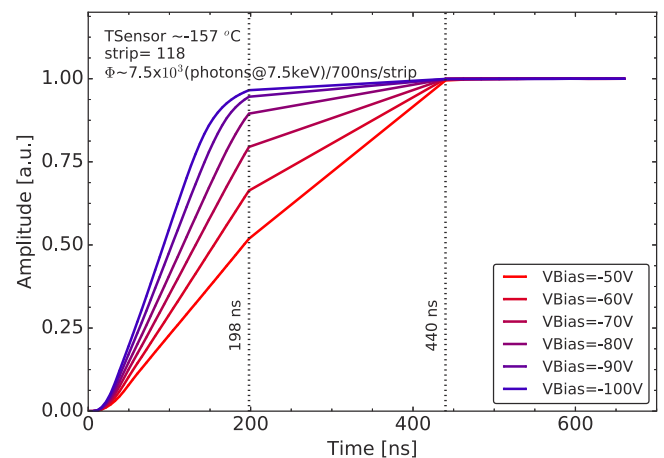
Fig. 12. Charge-collection as a function of time for different bias voltages, at a constant X-ray intensity.
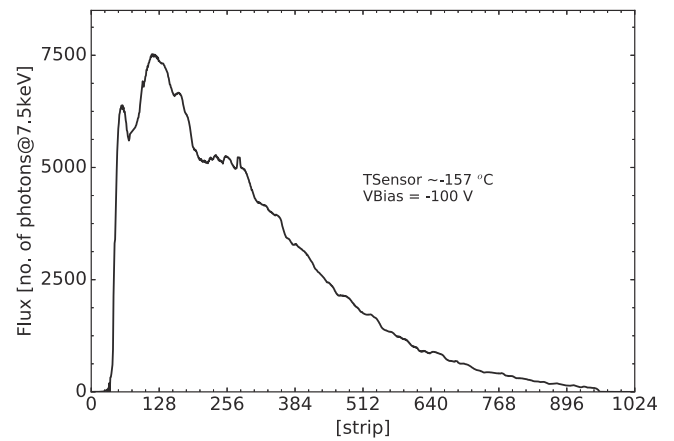
the integration time was scanned from 0 ns to 198 ns in steps of 5.5 ns, and from 440 ns to 638 ns in steps of 22 ns. The region between 198 ns and 440 ns was not sampled. The curves were normalised to the ADU value at 638 ns i.e the last sample. Pedestal subtraction was applied before normalisation.

It is observed in Fig. 11(b) that all signals are collected within 700 ns i.e. within the ∆t separating X-ray flashes in 4 bunch mode. The signal collection in the first 198 ns is affected by the intensity of the X-rays. It is slower to collect the charge ionised by a higher photon flux.
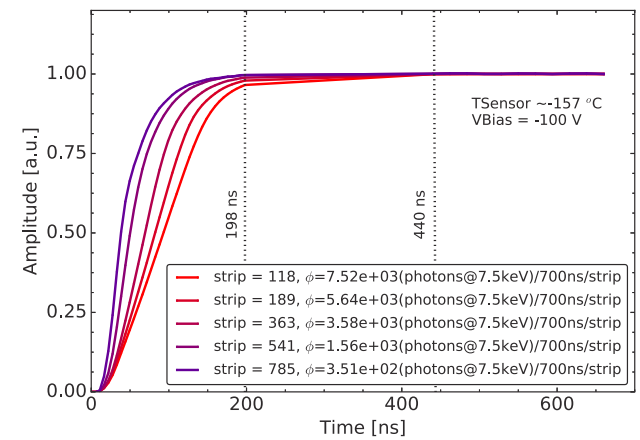
The effect of the bias voltage on the charge-collection for a high flux of ∼7500 photons at ∼7.5 keV is presented in Fig. 12. Six different voltages are compared, scanned from −50 V to −100 V in steps of 10 V. It is observed that a higher voltage increases the drift velocity inside the bulk, reducing the charge-collection time.

5.2. Test-run of a pump–probe experiment

A test-run was organised at ID24 to perform pump and probe experiments with prototype instrumentation. The set-up consisted of the second prototype cryostat of the XH detector, and the front-end assembly of the laser providing excitation pulses to the sample.

The representative case presented here consisted of a sample of Fe–wt10%Ni. The energy spectrum of the sample was first measured in ambient conditions, by averaging about 10 sequential X-ray pulses.
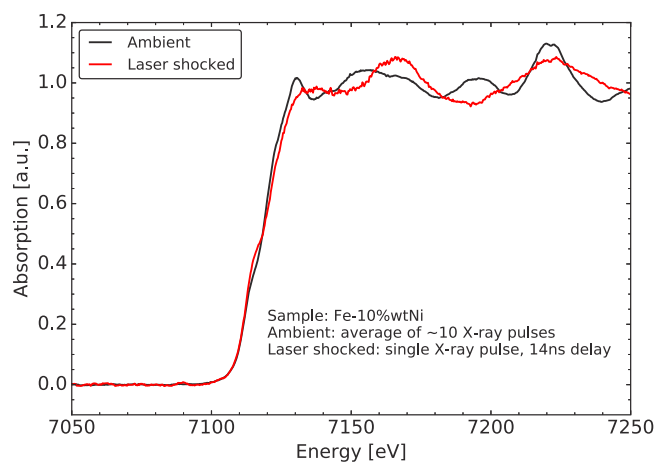
Fig. 13. Comparison of energy dispersive spectra for a sample of Fe–wt10%Ni.

Then a laser pulse was shone onto the sample, giving rise to a shock wave. The pulse duration was 8 ns and it had an energy of 15 J. The laser pulse was focused to 250 μm (full width half maximum) at the sample position. One single X-ray pulse (100 ps) was used to acquire the spectrum for the laser shocked sample. This is because the excited sample is in a short-lived state (ns), requiring the fast data acquisition of a single X-ray pulse.

The two spectra are compared in Fig. 13. At ambient conditions, the spectrum shows the typical features of the body centred cubic structure. In the excited state, it is observed that the sample transitioned to an hexagonal closed packed structure.

These types of experiments are exploited by scientists to characterise chemical and physical processes in matter. The upgrade of the ESRF synchrotron to the EBS will provide brighter X-ray pulses, reducing photon statical noise on single shot measurements. Therefore improving the quality of the measurements.

6. Conclusion

The prototyping experience reported in this work included electrical and in-beam measurements on test structures and micro-strip sensors from two 1.5 mm thick Ge wafers. The aim was to validate the performance of this technology for EDXAS applications at ID24.

Test structures were CV tested to estimate a depletion voltage of ~25 V for a 1.5 mm thick bulk. A first sensor was installed into a prototype cryostat and stress-tested via temperature cycling testing. Sensor, electronics, interconnection and mechanics were able to withstand repeated temperature cycling (105 cycles) without showing a substantial change in their performance. Further reliability tests were implemented on this sensor post temperature cycling testing. The total leakage current was monitored for ~21 days at −175 V at a temperature of ~−173 °C without showing any run-away behaviour. In addition, 50 sequential IVs were measured on the sensor at a hotter temperature of −155 °C showing a good repeatability. A temperature scan on the sensor showed the leakage current decreasing at lower temperatures as expected.

A second sensor was installed into a second cryostat and it was in-beam tested at ID24 before the long shut-down of the synchrotron for the EBS upgrade. Here, charge-collection was measured as a function of time at different X-ray fluxes and bias voltages. Charge was always collected within the 700 ns. X-ray intensity and bias voltage affect charge-collection in the first 198 ns.

A test-run of an experiment was performed with the pump and probe technique. An experimental sample (Fe–10%wtNi) was laser shocked and its structural transition successfully recorded.

Results were deemed satisfactory and the project will progress by building two production cryostats for the XH system, instrumented with these sensors.

CRediT authorship contribution statement

M. Borri: Formal analysis, Project administration, Funding acquisition, Visualization, Methodology. **C. Cohen:** Investigation. **J. Groves:** Project administration, Funding acquisition, Investigation, Methodology. **W. Helsby:** Formal analysis, Funding acquisition, Visualization, Investigation, Methodology. **O. Mathon:** Conceptualization, Funding acquisition. **L. McNicholl:** Investigation, Methodology. **S. Pascarelli:** Conceptualization, Funding acquisition. **N. Sévelin-Radiguet:** Investigation. **R. Torchio:** Conceptualization, Funding acquisition. **M. Zuvic:** Investigation, Methodology.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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